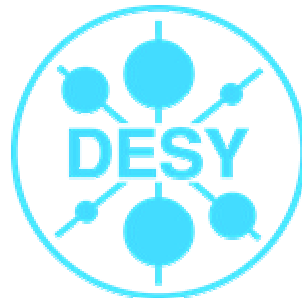


Third generation LLRF Control System Development

WORK STATUS

Speaker: Waldemar Koprek

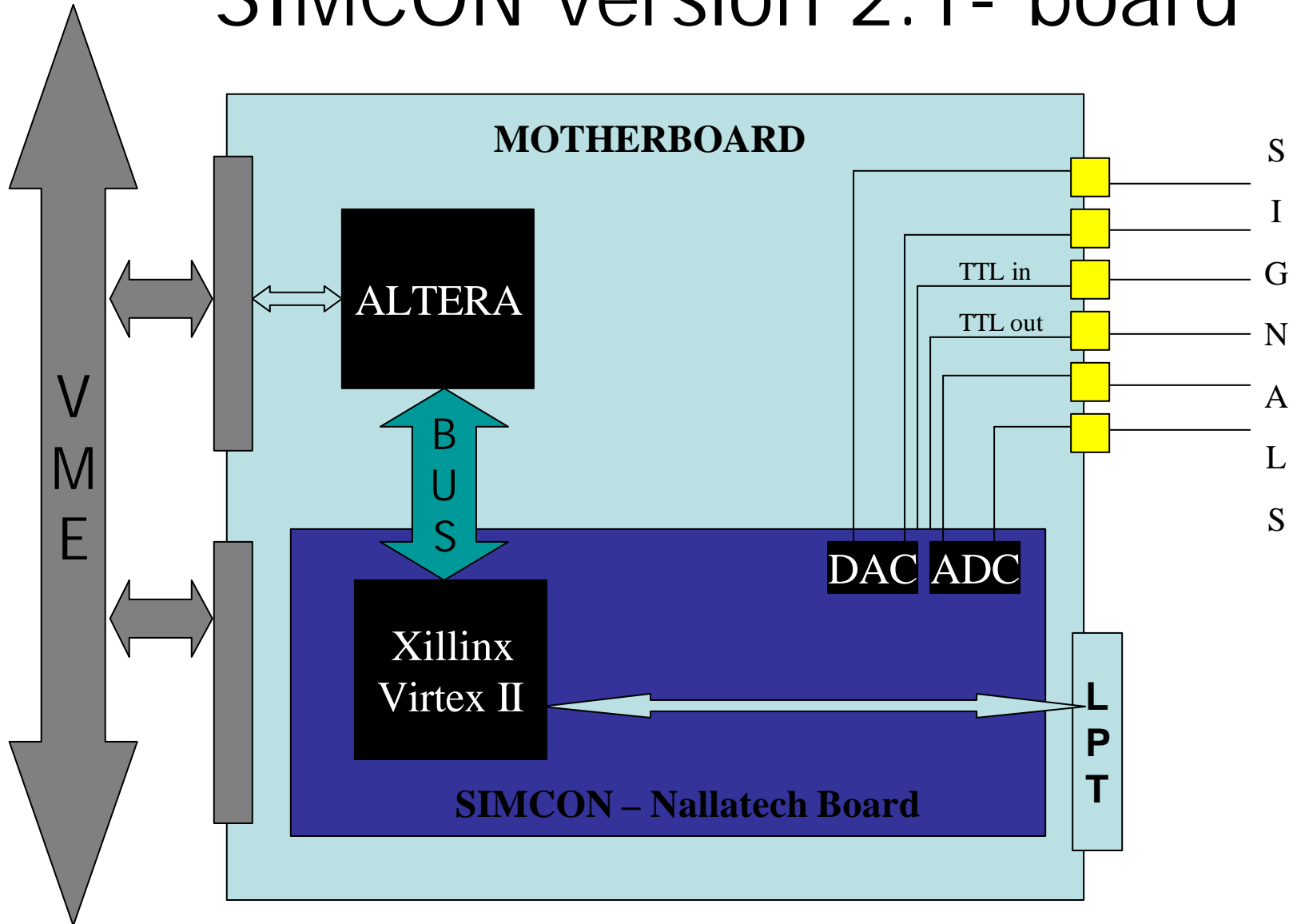


SIMCON version 2.1 – features

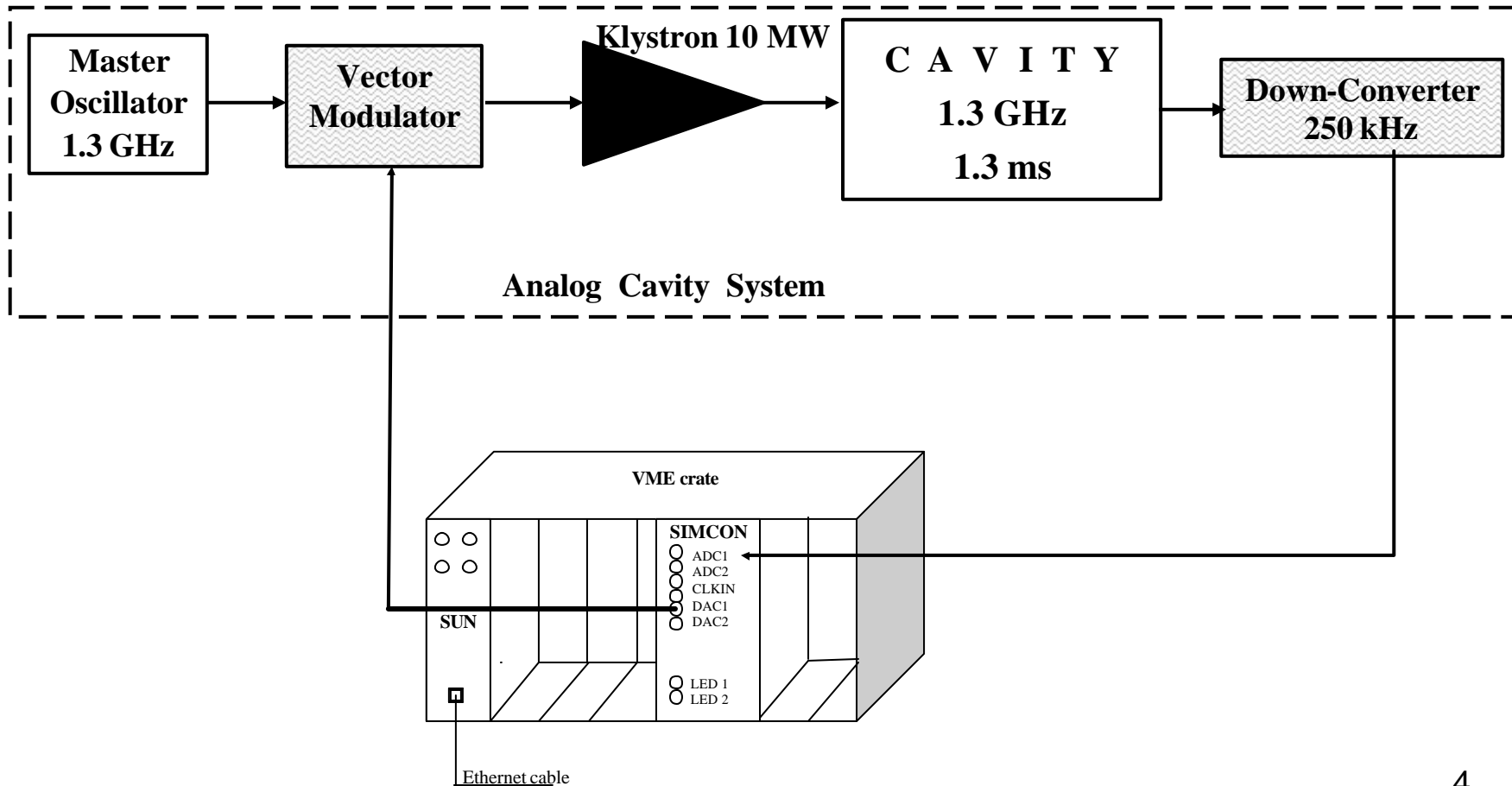
(real time mode operation)

- **Hardware:**
 - FPGA chip – Xilinx Virtex II 3000
 - 2xADC
 - 2xDAC
 - Motherboard with LPT, VME interfaces
 - Internal and external clock system (compatible with LLRF timing system)
- **Software:**
 - cavity simulator
 - cavity controller
 - control algorithm in Matlab
 - laboratory software for Matlab & DOOCS
 - Matlab & DOOCS control interfaces

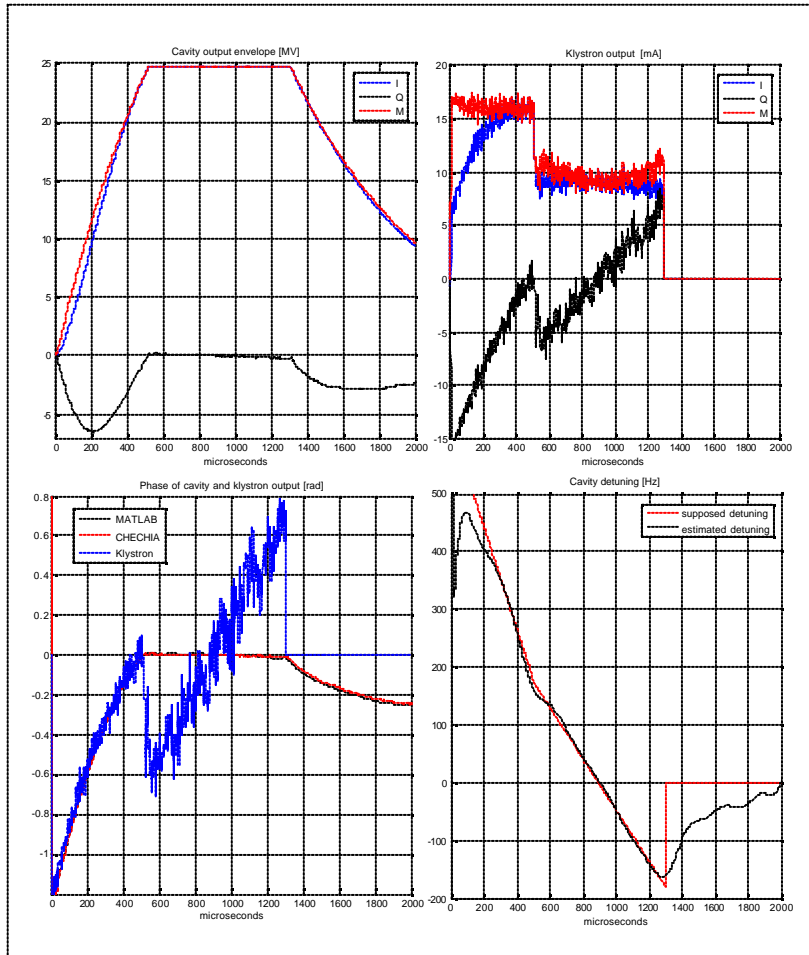
SIMCON version 2.1- board



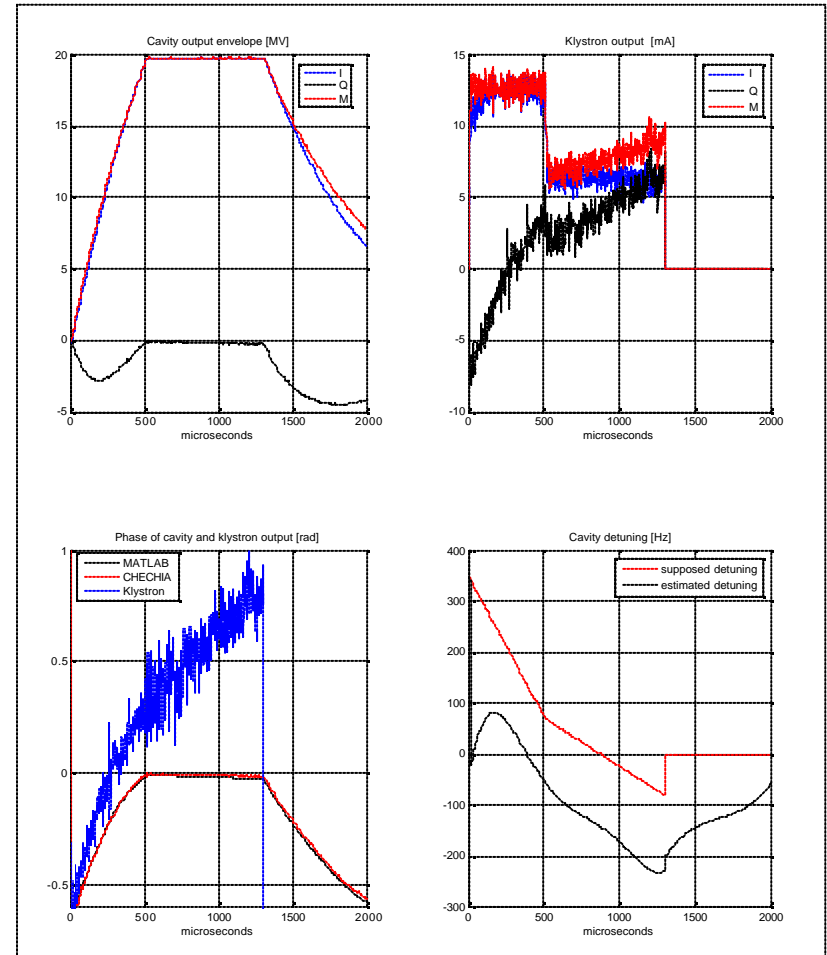
SIMCON version 2.1- tests



SIMCON version 2.1- results



Feedback cavity driving (gain = 100):
selected readout for 25 MV *flattop* level



Feedback cavity driving (gain = 100):
selected readout for 20 MV *flattop* level

SIMCON version 3 – features

(multichannels real-time version)

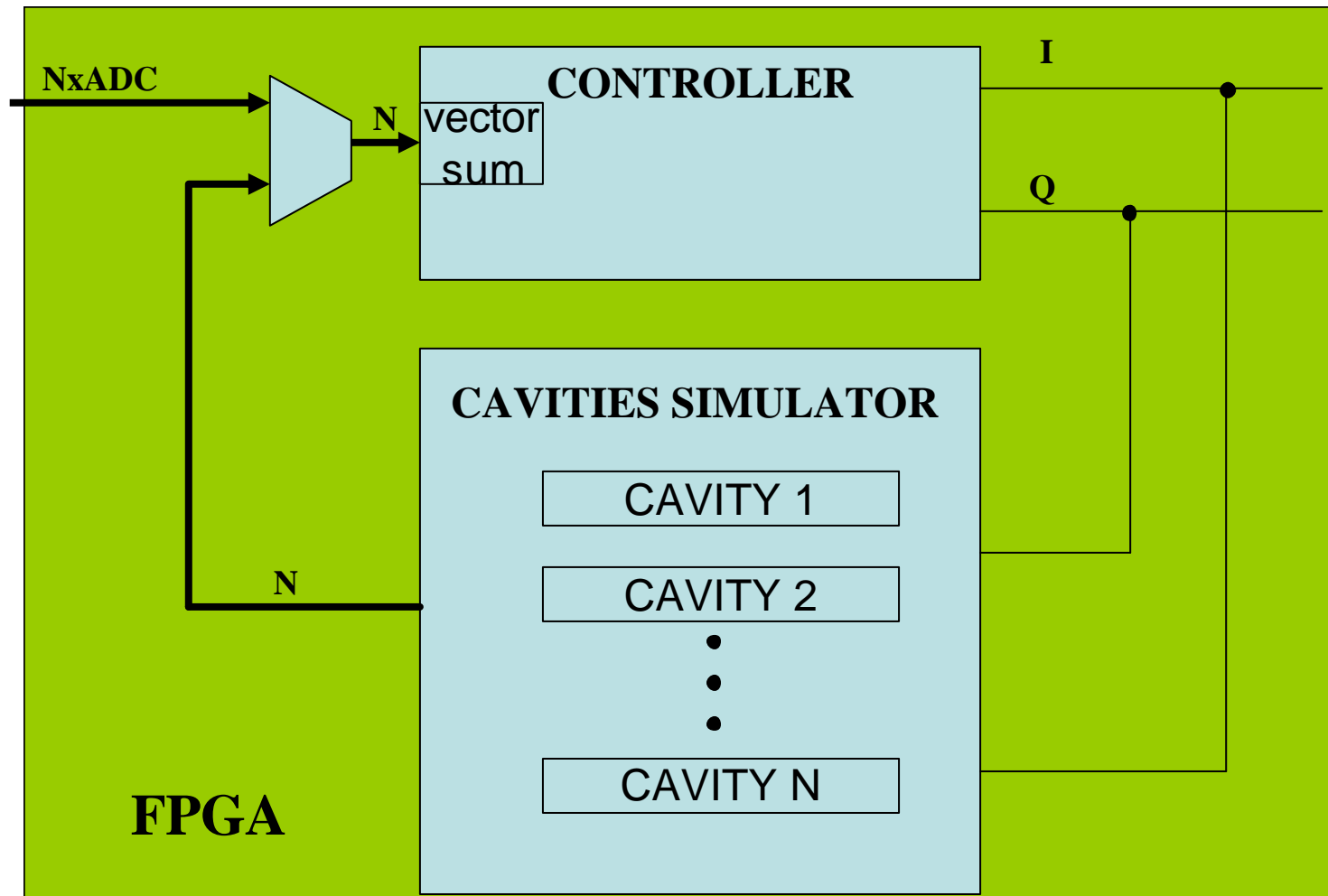
- **Hardware:**
 - FPGA chip – Xilinx Virtex II 4000
 - 8xADC
 - 4xDAC
 - Internal and external clock system
 - Universal motherboard
- **Mezzanine boards**
 - VME interface with Altera ACEX chip (A24D32)
 - PC embedded Etrax with Ethernet (100T)
 - Optical transfer 2.5Gb (two transceivers)

SIMCON version 3 - software

- Multi inputs controller
 - channel with rotation and scaling matrix
 - monitoring data from each channel
 - vector sum (channel enabling)
- Multi cavities simulator
 - rotation and scaling matrix for each channel

SIMCON version 3

FPGA architecture



SIMCON version 4

or

Low Latency Control Board

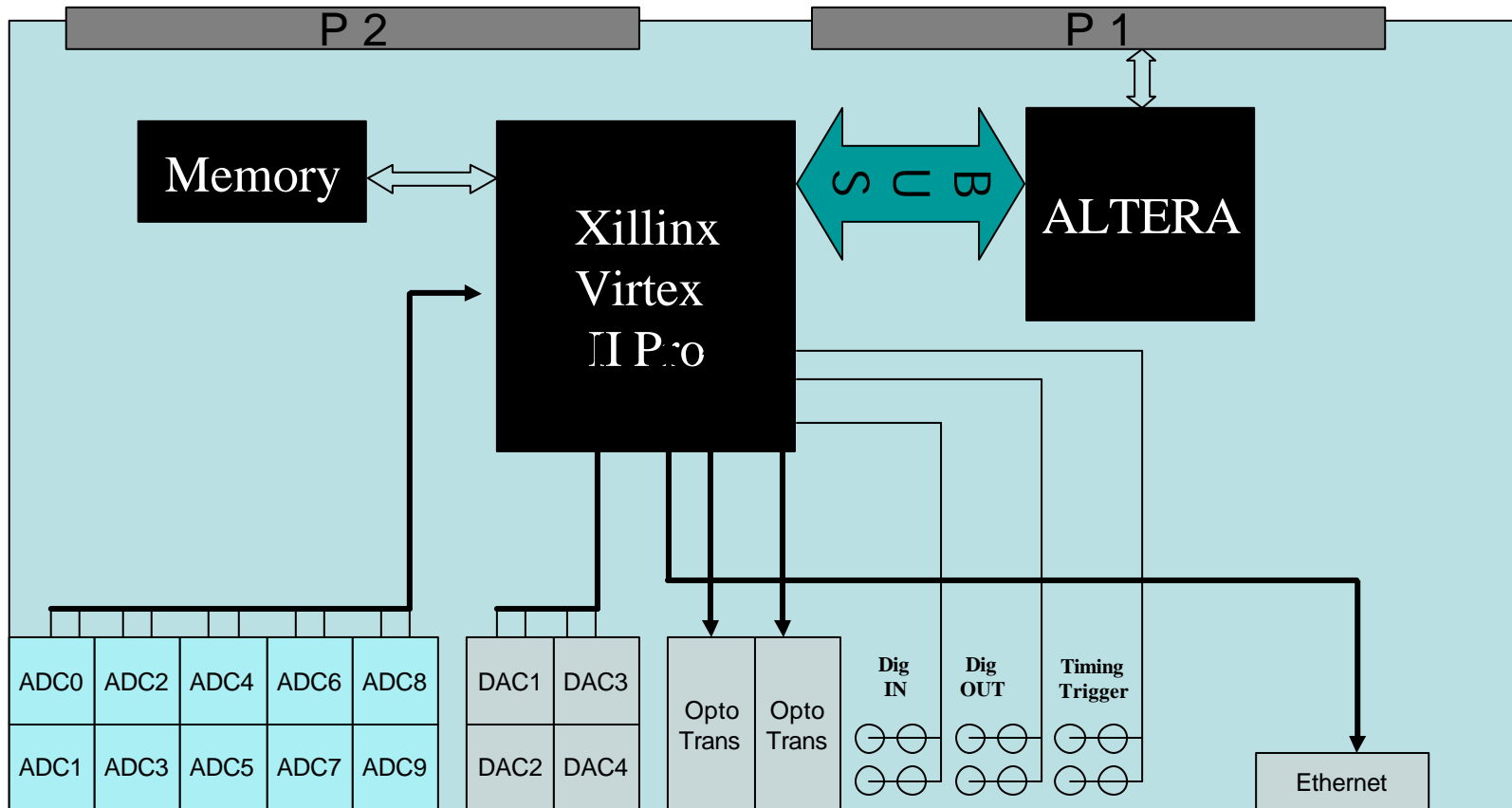
Hardware requirements:

- 10 x ADC, 14-bits, sampling frequency > 100 MHz
- 4 x DAC, 14-bits, sampling frequency > 100 MHz
- 4 (minimum 2) optical transceivers
- Vitrex II Pro FPGA
- external memory in one chip (2MB)
- 4 digital inputs
- 4 digital outputs
- input for a timing signals (1x clock, 3x trigger)
- optical input for timing (9MHz with event coding)
- VME interface
- size of the board 6U (standard DOOCS crate)
- Ethernet 10 Mbit/s (or 100 Mbit/s ?)

SIMCON version 4

or

Low Latency Control Board



SIMCON version 4

or

Low Latency Control Board

- Rough schedule
 - 1 week for work arrangement
 - 3 weeks for schematics
 - 1.5 month for PCB
 - 2 weeks for possible Delay
 - 1 month for production
 - running and testing board